TS128MFB72V5J-T

240PIN DDR2 533 Fully Buffered DIMM
1GB With 64Mx8 CL4

_Description

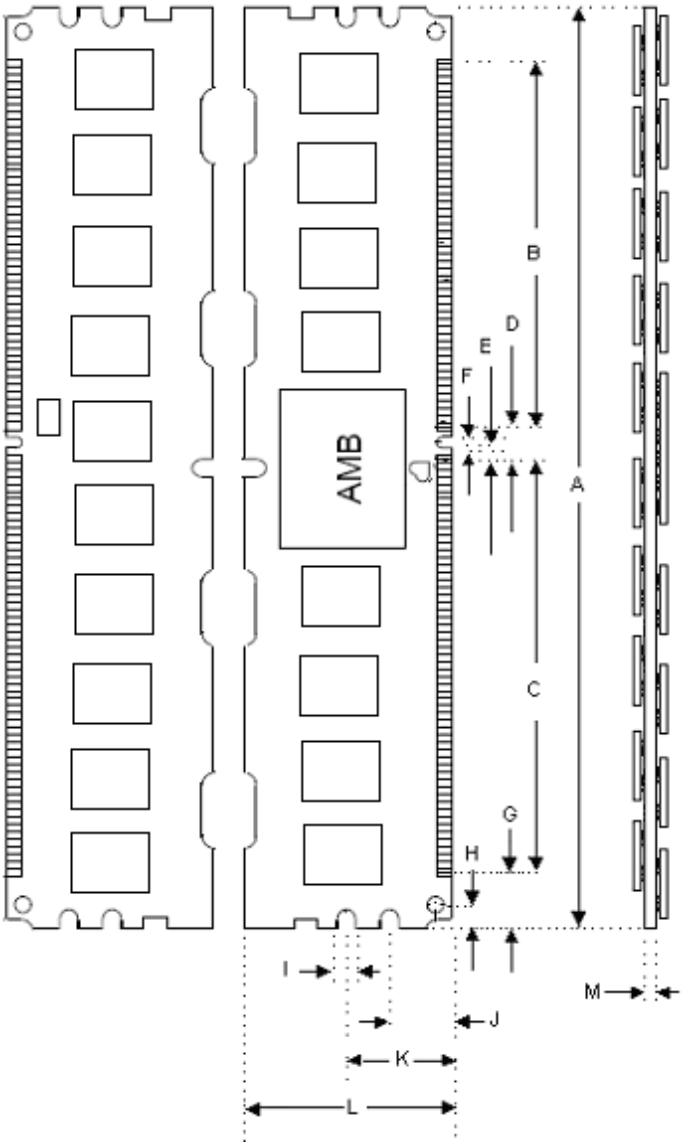
The TS128MFB72V5J-T is a 128M x 72bits DDR2-533 Fully Buffered DIMM. The TS128MFB72V5J-T consists of 18pcs 64Mx8bits DDR2 SDRAMs in 60 ball FBGA package, 1 pcs AMB IC, and a 2048 bits serial EEPROM on a 240-pin printed circuit board. The TS128MFB72V5J-T is a 240pin fully buffered dual in-line memory module.

The Advanced Memory Buffer also allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the memory channel. Fully Buffered DIMM provides a high memory bandwidth, large capacity channel solution that has a narrow host interface.

Features

- 240pin fully buffered dual in-line memory module
- 3.2Gb/s, 4.0Gb/s link transfer rate
- 1.8V +/- 0.1V Power Supply for DRAM VDD/VDDQ
- 1.5V +/- 0.075V Power Supply for AMB VCC
- 3.3V +/- 0.3V Power Supply for VDDSPD
- Buffer Interface with high-speed differential point-to-point Link at 1.5 volt
- Channel error detection & reporting
- Channel fail over mode support
- Serial presence detect with EEPROM
- 4 Banks
- Posted CAS
- Programmable CAS Latency : 3, 4, 5
- Automatic DDR2 DRAM bus and channel calibration
- MBIST and IBIST Test functions
- Hot add-on and Hot Remove Capability
- Transparent mode for DRAM test support

Placement



PCB: 09-2600

Dimensions

Side	Millimeters	Inches
A	133.35±0.15	5.250±0.006
B	51	2.0
C	67	2.64
D	5	0.197
E	2.5	0.098
F	1.5±0.10	0.059±0.039
G	5.175	0.204
H	3.25	0.128
I	3	0.118
J	9.5	0.374
K	18.8	0.74
L	30.35±0.15	1.2±0.006
M	1.27±0.10	0.050±0.004

(Refer Placement)

Pin Description

Symbol	Function
SCK	System Clock Input, positive line
/SCK	System Clock Input, negative line
PN[13:0]	Primary Northbound Data, positive lines
/PN[13:0]	Primary Northbound Data, negative lines
PS[9:0]	Primary Southbound Data, positive lines
/PS[9:0]	Primary Southbound Data, negative lines
SN[13:0]	Secondary Northbound Data, positive lines
/SN[13:0]	Secondary Northbound Data, negative lines
SS[9:0]	Secondary Southbound Data, positive lines
/SS[9:0]	Secondary Southbound Data, negative lines
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input / Output
SA[2:0]	SPD Address Input, also used to select the DIMM number in the AMB
VID[1:0]	Voltage ID: these pins must be unconnected for DDR2-base Fully Buffered DIMMs VID[0] is VDD value:OPEN=1.8V,GND=1.5V VID[1] is Vcc value:OPEN=1.5V,GND=1.2V
RESET	AMB reset signal
RFU	Reserved for Future Use
VCC	AMB Core Power and AMB Channel interface Power (1.5 Volt)
VDD	DRAM Power and AMB DRAM I/O Power (1.8 Volt)
VTT	DRAM Address/Command/Clock Termination Power (VDD/2)
VDDSPD	SPD Power
VSS	Ground
DNU/M_Test	The DNU/M Test pin provides an external connection R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected(DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VDD	41	/PN13	81	VSS	121	VDD	161	SN13	201	VSS
02	VDD	42	VSS	82	PS4	122	VDD	162	VSS	202	SS4
03	VDD	43	VSS	83	/PS4	123	VDD	163	VSS	203	/SS4
04	VSS	44	RFU**	84	VSS	124	VSS	164	RFU**	204	VSS
05	VDD	45	RFU**	85	VSS	125	VDD	165	RFU**	205	VSS
06	VDD	46	VSS	86	RFU**	126	VDD	166	VSS	206	RFU**
07	VDD	47	VSS	87	RFU**	127	VDD	167	VSS	207	RFU**
08	VSS	48	PN12	88	VSS	128	VSS	168	SN12	208	VSS
09	VCC	49	/PN12	89	VSS	129	VCC	169	/SN12	209	VSS
10	VCC	50	VSS	90	PS9	130	VCC	170	VSS	210	SS9
11	VSS	51	PN6	91	/PS9	131	VSS	171	SN6	211	/SS9
12	VCC	52	/PN6	92	VSS	132	VCC	172	/SN6	212	VSS
13	VCC	53	VSS	93	PS5	133	VCC	173	VSS	213	SS5
14	VSS	54	PN7	94	/PS5	134	VSS	174	SN7	214	/SS5
15	VTT	55	/PN7	95	VSS	135	VTT	175	/SN7	215	VSS
16	VID1	56	VSS	96	PS6	136	VID0	176	VSS	216	SS6
17	/RESET	57	PN8	97	/PS6	137	DNU/M_Test	177	SN8	217	/SS6
18	VSS	58	/PN8	98	VSS	138	VSS	178	/SN8	218	VSS
19	RFU**	59	VSS	99	PS7	139	RFU**	179	VSS	219	SS7
20	RFU**	60	PN9	100	/PS7	140	RFU**	180	SN9	220	/SS7
21	VSS	61	/PN9	101	VSS	141	VSS	181	/SN9	221	VSS
22	PN0	62	VSS	102	PS8	142	SN0	182	VSS	222	SS8
23	/PN0	63	PN10	103	/PS8	143	/SN0	183	SN10	223	/SS8
24	VSS	64	/PN10	104	VSS	144	VSS	184	/SN10	224	VSS
25	PN1	65	VSS	105	RFU**	145	SN1	185	VSS	225	RFU**
26	/PN1	66	PN11	106	RFU**	146	/SN1	186	SN11	226	RFU**
27	VSS	67	/PN11	107	VSS	147	VSS	187	/SN11	227	VSS
28	PN2	68	VSS	108	VDD	148	SN2	188	VSS	228	SCK
29	/PN2	69	VSS	109	VDD	149	/SN2	189	VSS	229	/SCK
30	VSS	70	PS0	110	VSS	150	VSS	190	SS0	230	VSS
31	PN3	71	/PS0	111	VDD	151	SN3	191	/SS0	231	VDD
32	/PN3	72	VSS	112	VDD	152	/SN3	192	VSS	232	VDD
33	VSS	73	PS1	113	VDD	153	VSS	193	SS1	233	VDD
34	PN4	74	/PS1	114	VSS	154	SN4	194	/SS1	234	VSS
35	/PN4	75	VSS	115	VDD	155	/SN4	195	VSS	235	VDD
36	VSS	76	PS2	116	VDD	156	VSS	196	SS2	236	VDD
37	PN5	77	/PS2	117	VTT	157	SN5	197	/SS2	237	VTT
38	/PN5	78	VSS	118	SA2	158	/SN5	198	VSS	238	VDDSPD
39	VSS	79	PS3	119	SDA	159	VSS	199	SS3	239	SA0
40	PN13	80	/PS3	120	SCL	160	SN13	200	/SS3	240	SA1

RFU = Reserved Future Use

* These pin position are reserved for forwarded clocks to be used in future module implementations

** These pin positions are reserved for future architecture flexibility